# JAGUAR CD ROM DRIVE MODULE

# TEST SPECIFICATION

# October 20   1994.

## SECRET AND CONFIDENTIAL

# 1.0   Overview

This  document  describes  various  test  procedure  and  specifications  which  must  be
run in   production. It  is  referred  to  by  various  test  and  QA  documents  from  time
to time  including  the  acceptance  specification

**Section 2**  describes  the   requirements  for  in-circuit  test - the  primary  tool  for
identifying  and  controlling  manufacturing  costs.

**Section 3**  describes  the  requirements  for  Static  Burn-in  test

**Section 4** describes  the  requirements  for  PCBA  functional  test - designed  to  check
all  system  functions  and  provide  diagnostic  information  for  systems  which  do  not
perform  as  required.


**Section 6**  describes the tests that can be  used for diagnosis of failed PCBA's.

**Section 7**   shows the complete test flow chart


**Appendix A**  describes the specification for  building the PCBA Functional test fixture

**Appendix B**  describes the Static Burn-in test specification.

# 2.0   In - Circuit - Test

## 2.1   Equipment / Setup

**Equipment  Required:**

The  manufacturer  is  responsible  for  selecting  the  equipment,  building fixtures
and  generating  the  in-circuit  test  program. The  manufacturer  must  provide Atari  with  a  summary  of  tests  performed  on  each  components,  including  the level  of  coverage,  tolerances,  and  a  list  of  components  not  tested. Additional function  tests may  be  required  depending  on  the  level  of  testing  achieved at
in-circuit test.

**Unit Under Test:**

APN   700037        Jaguar CD ROM Drive Printed Circuit Assembly.

**Test Condition:**

Temperature:      25 degree C  +/-   4 degree C

**Setup:**

Set UUT on ICT fixture and start test,

## 2.2  Shorts Test

A shorts test  must be  performed  on  all  nodes  accessible  to  the  test  fixture. Any node  not  included  in  the  shorts  test  must be  summarized  and  reported  to  Atari.

## 2.3  Analog Passive Parametric Test

A  parametric value  test  must  be  performed  on   all analog  passive components
individually  accessible. Values  and  tolerances  should  match  the  bill  of materials,
Parallel analog  passive components should  be  tested  in  parallel. Any analog
passive  components  not  tested  must  be  summarized  and  reported  to  Atari.

## 2.4  Active Devices Test

Each input pin on active analog and digital devices must be driven/state toggled
while the device is powered  and  level/state  changes received on each device
output pin. Any device not 100% tested must be  summarized and  reported to Atari.

## 2.5  Frequency Test

Crystals X1 and X2 must be measured to better than 0.0025%

## 2.6  Memory Test

A CRC  and  checksum test  of  the  8bit ROM  must  be  provided.

## 2.7  Voltage  Test

Verify  Supply  Voltage  at  TP337 (Pin 5 of U5)  and  GND (Pin 3 of U13)
= **5V DC  +/-0.050V**

Verify  Supply  Voltage  at  TP334 ( Pin 5 of U5) and  GND (Pin 3 of U13)
= **7V DC  +/-0.050V**

Verify Voltage at TP35 (Pin 9 & 10 of U8) and GND (Pin 12 of U8)
= **2.50V DC +/- 5%**

Verify Voltage at TP89 (Pin 14 of U4) and GND (Pin 15 of U4)
= **1.15V DC  to  1.31V DC**

Verify Voltage at TP88 (Pin 4 of U3) and GND (Pin 21 of U3)
= **1.35V DC  +/- 10%**

Verify Voltage at TP23 (Pin 7 of U1) and GND (Pin 14 & 10 of U1)
= **2.50V DC  +/- 5%**

## 2.8  Custom ASIC's

Custom  ASIC's  are  fully  tested  at  the  vendor. The  preferred  Atari  method  for  checking  opens  is  HP Test Jet  on  the   HP 3070.

### 2.9   Reports

A variety of weekly reports must be provided:
- a.  Overall yield and first pass yield ( boards must be serialized),
- b.  Failure Pareto charts identifying top 10 failing tests.
- c.  Repair Pareto charts identifying top 10 component repairs.

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# 3.0  Static  Burn-in  Test

This test is conducted in a burn-in rack, with  power  applied  to  PCBA  and without  exercising any  software. This  test  is  conducted  on  all  production unit.

## 3.1  Equipment / Setup

**Equipment Required:**

Interconnect  PCBA  with  5V DC Supply voltage
Power Distribution Network
Burn-in  facility
High Capacity Dual Voltage Power Supply (+9VDC,  +5VDC)

**Unit Under Test:**

APN   700037        Jaguar CD ROM Drive Printed Circuit Assembly.

**Test  Condition:**

Temperature :   50 degree C

**Setup:**

Set  UUT  in  the  burn-in rack
Apply  9VDC  to  UUT  power  jack.
Apply  5VDC  to  UUT  through  interconnect  PCBA.
Set  burn-in  rack  temperature to  50 degree C.

**Burn-in:**

The UUT with 9VDC and 5VDC power applied, will remain in the burn-
in

rack for a period of 8hrs. At the end of 8hrs, the PCBA functional test is
performed on the UUT.

# 4.0  PCBA  FUNCTIONAL  TEST

This test is required on 100% of all production.

## 4.1  Equipment / setup

**Equipment required:**

Manufacturer must provide a bed of nails test fixture that contains a
Jaguar console containing test software and a known good CD ROM DRIVE
(CDM 12) mechanism with an Atari Test CD mounted. The UUT and Jaguar
console are powered by Atari AC wall plug adapters. The Jaguar console is
connected to an IBM PC serial port with a custom Jaguar serial data cable
software running on the Jaguar console starts and stops the mechanism as
required by the tests. The test is approximately 2 minutes and 20 seconds long.

Atari CD ROM Test Disc
AC wall plug power adapter ( 2 required )
Suite 2 Test Software.
Custom Jaguar serial data cable.
IBM PC
Leader LJM 1851 CD Jitter Meter

**Unit Under Test:**

APN 700037    Jaguar CD ROM DRIVE PCB assembly.

**Test Conditions:**

Temperature:    25 degree C +/-  4 degree C
Humidity:        25% to 70% relative humidity

**Setup:**

Set UUT on the test fixture
Connect UUT to Jaguar console PCBA via CD ROM extender card.
Connect CD ROM DRIVE Mechanism to UUT.

Place Atari Test CD on the  CD ROM DRIVE Mechanism.
Connect AC adapter to UUT  power jack.
Connect AC adapter to Jaguar console PCBA.
Connect  Jaguar PCBA  to  IBM PC  serial  port  via  a custom  Jaguar
                                                          serial data cable..
Power ON to start the test software on the Jaguar Console PCBA.
The terminal displays the message
            **"Please wait for sanity check to complete"**

If the sanity check passes the terminal will display the message
            **" Quick check passed.  Starting PCBA tests "**

 The automated test series begins at this point
 The automated test series checks the following:
                EEPROM  write / read back
                FFFF/0000 words serial data test
                Dual counter serial data test        and
                Butch FIFO to Tom 32-bit data test.
  At the end of a successful test series the terminal displays the message
            **" UUT self test passed   Congratulations"**
            **" External evaluation required for the following tests"**
  At the end of each measurement type any key on the PC to begin the next test.
  .


### 4.4.5  Block error rate (BLER) at  inner and outer diameters of disc
            **Note:** To perform this test, the UUT should have the following
modification

        a)  The jumper link at JP225 should be between pins 2 and 3.
        b)   Pin 2 of  JP 210 ( BTCH V4)  should  be  pulled high to VCC  by
                                            a pull up resistor ( 4.7K 1/4W)


        This  automated test  measures  BLER  on  the  inner  and  outer  tracks  of
        the Atari  Test  Disc, at  double speed.  As  the test proceeds, the  message
                **BLER count was  $xxxx**
        This message appears 8 times
        The test operator has to inspect the BLER count and determine if the
        PCBA  has passed or failed the BLER test.
    All BLER counts  less than $0064   ------------   PCBA **passed** the BLER test
    Any BLER count  greater than $0064 ---------    PCBA **failed** the BLER test

### 4.3  Complete  System  Voltage and Current Test:

#### 4.3.1  Power Supply current ( measured at the supply point )

On the power cord, near the power input jack on the CD  ROM PCB,
measure the input current
Should be = **111 mA. +/-  10 mA**

#### 4.3.2  Power Supply current draw after regulator U5 (+5V)

Measured between JP224 Pin 1(TP9) and JP224 Pin 2 (TP337)
Should be between **55 to 65 mA**.

#### 4.3.3  Power Supply current draw after regulator  U13 (+7V)

Measured between JP223 Pin 1(TP63) and JP223 Pin 2 (TP334)
Should be between  **24  to  30  mA.**
Note that this is the value "C" used below.

#### 4.3.4  Laser Current

Voltage at TP60 (R24), focus off = (your measurement A)
Voltage at TP60 (R24), focus  on = (your measurement B)
Calculate  current: $I_{laser}$ = (B-A) / 4.7
Verify that $I_{laser}$ <  **76 mA.**

#### 4.3.5  Focus Current

Measure current between JP223 Pin 1(TP63) and JP223 Pin 2 (TP334)
$$= \text{'D' mA}$$
Calculate current:  $I_{focus}$ =  D - C
Verify that $I_{focus}$ **< 50 mA**

#### 4.3.6  Spindle motor current at double speed

With the test CD spinning at double speed in the drive, focus and radial off,
measure current between JP223 Pin 1(TP63) and JP223 Pin 2 (TP334)
$$= \text{'F' mA}$$

Calculate current :  $I_{spindle\ 2}$ =  F - C
Verify that $I_{spindle\ 2}$ **< 60 mA**

#### 4.3.8  Peak Hold current

As  the  test  software starts and stops the drive repeatedly, measure the peak
current between JP223 Pin1(TP63) and JP223 Pin 2(TP334).
Verify that $I_{peak}$ **< 1000 mA each time**.

## 4.5    Behavior of spindle motor

These tests are performed with the disc spinning at double speed.

### 4.5.1  Spindle motor DC voltage at inner diameter of disc
Measure the DC voltage between pin 3 (TP362) and pin 4 (TP363) on JP4 (motor cable connector) and verify that...

$V_{motor\ DC}$ =  **1.18 Volts, +/- 20%**

### 4.5.2  Spindle motor RMS voltage at inner diameter of disc
Measure the RMS voltage between pin 3 (TP362) and pin 4 (TP363) on JP4 (motor cable connector) and verify that...

$\mathbf{V_{motor\ RMS}}$  =  TBD Volts, +/- 20%

### 4.5.3  Spindle motor DC voltage at outer diameter of disc
Measure the DC voltage between pin 3 (TP362) and pin 4 (TP363) on JP4 (motor cable connector) and verify that...

$V_{motor\ DC}$ = **0.66Volts, +/- 20%**

### 4.5.4  Spindle motor DC voltage at outer diameter of disc
Measure the RMS voltage between pin 3 (TP362) and pin 4 (TP363) on JP4 (motor cable connector) and verify that...

$V_{motor\ RMS}$ = **TBD Volts, +/- 20%**

## 4.4   HF Signal Quality Measurement:
The high frequency RF signal input to the Philips 7345 decoder is measured with
a Leader LJM 1851 CD Jitter Meter and Jaguar self test software block error (BLER) counter.
Connect Jitter Meter probe to TP34 and ground to TP345 (Pin 1 of JP219) of the UUT.
Turn ON the Jitter Meter. The Jitter Meter setup should be as follows:

$$\textbf{LEVEL} : \quad \text{Range(V}_{pp}) \quad \text{--} \quad 1.5\text{V}$$

$$\text{Bit} \quad \text{------------} \quad 3\text{T Bits}$$

$$\textbf{JITTER} : \quad \text{Response ------} \quad \text{Sigma}$$

$$\text{Range ---------} \quad 60 \text{ nS range}$$

$$\text{Polarity --------} \quad \text{Inverted}$$

## 4.4.1 & 4.4.2 $I_3$ Voltage P-P and Jitter at disc ID

Verify that $I_3 = \textbf{1.05 Volts P-P +/- 20\%}$

Verify that **Jre < 32 nanoseconds**

## 4.4.3 & 4.4.4 $I_3$ Voltage P-P and Jitter at disc OD

Verify that $I_3 = \textbf{1.05 Volts P-P +/- 20\%}$

. Verify that **Jre < 32 nanoseconds**

If the complete test series is successful, the terminal will display the message.

**"UUT test Complete"**

. **"UUT self test passed, Congratulations"**

The terminal then display the following messages

**Main Menu**

**(B)**    **BLER tests, Needs JP225 and 4.7K resistor**
**(C)**    **Current and voltage tests on PCBA**
**(D)**    **Data integrity tests using Jerry , then Tom**
**(E)**    **EEPROM write and read back test**
**(F)**    **Film clip endless-loop playback**
**(H)**    **Hole-in CD tolerance test, Needs SBC444A CD**
**(J)**    **Jitter tests**
**(R)**    **RW Sub codes for CD + Graphics tests**
**(S)**    **Seeks of decreasing Spans tests**

**Waiting......**

The test operator can select any test in the menu by the letter. Test selection from the Main Menu becomes necessary only when the UUT fails the initial test series and the test operator wants to repeat a failed test. The test software in the Jaguar console runs the selected test and the terminal displays the Main Menu enabling the test opertor to select any other test in the

menu.

## 5.0   Final Systems test

This is  an  automated  functional  test  series  performed on  the  device  under test.

During  the  test,  the  TV   screens  remains   blue.  If  the  test  ends  successfully, the  screens  turns  green.  Any   failure  of  the  device  under  test  causes  the  test software ( residing in  the  test  cartridge ) to  make  the  TV  screens turn  red  and exit  the  test.  The  duration  of  the  test series  is  less than 1.5  minutes.

### 5.1  Equipment / Setup

**Equipment Required:**

>       Jaguar  game  console (2 units)
>       Suite 1 Test  cartridge A
>       Suite 1 Test  cartridge B
>       Suite 1 Test  CD  ROM
> .     AC  Power Adapter  ( 4  required )
>       Jaguar joystick mating connector with
>                       tricolor (red,yellow,green) L.E.D  ( 2 required)
>       Jaguar CD ROM Player PCBA (modified for BLER measurment)
>                                    in  bottom case.

**Unit  Under  Test:**

APN  800016-001     Jaguar  CD ROM DRIVE Console

**Test  Conditions:**

Temperature:     25 degree C  +/-   4 degree C
 Humidity:          25% to 70% relative humidity

**Setup:**

Refer setup diagram  for reference.
Mount UUT on  Jaguar game console A.
Insert the Suite 1 test Cartridge A into  the  game cartridge port of the UUT.
Connect  the  first  connector   with  tricolor  L.E.D  to joystick  port 1  of Jaguar
game console A.
Mount Jaguar CD ROM Player PCBA on Jaguar game console B.
Insert the Suite 1 test  Cartridge B  into  the  game  cartridge  port  of  the
CD ROM player PCBA.
Connect  the  second  connector with tricolor  L.E.D  to joystick  port 1  of  Jaguar
game console B.
Connect AC adapter to power jacks of Jaguar game consoles A and B.

Connect  AC  adapter  to  UUT  power  jack.
Connect  AC  adapter  to  CD  ROM  player  PCBA  power  jack.
Lift  CD  cover  of  the  UUT , place  Suite1  CD  ROM  test  disk  and close cover.
Plug BLER signal and ground  wires from cartridge  A  into  the  BLER  measuring
terminals on the CD ROM player PCBA (modified for BLER measurement)
mounted on Jaguar console B.

## 5.2  Test Description:

Power  up  the  Jaguar  consoles  A  and  B  simultaneously  by  pressing  the  red
switch on the Jaguar consoles.
Observe  the  yellow  L.E.D  flash  on Jaguar console A as the test series begins.
Wait for  green or red  L.E.D to light up on the Jaguar consoles A and B.
 If  Green L.E.D  lights up on  Jaguar consoles  A  and  B, it  indicate  the  UUT  has
PASSED the test series.
 If  Red  L.E.D  lights  up on  Jaguar  consoles A  and B, it  indicates  the  UUT has
FAILED the test series.
Turn off the UUT power.
Turn off the CD ROM PCBA power.
Turn off power to Jaguar consoles A and B .
Open cover of the UUT and remove CD ROM test disk.
Remove Test Cartridge from  UUT.
Remove UUT from Jaguar console.

### 5.4  Mechanical / Cosmetic  Inspection

The following  mechanical/cosmetic items  inspection  shall  be  done  at  final test

and during the final assembly stages.

No  missing  screws
No loose internal parts
No unacceptable molding defects in plastic case
No scratches, dirt, or finger prints on case
CD ROM drive mechanism  properly clamped to PCA
Correct serialized rating label in place
Correct Laser Safety label in place
Correct Class 1 Laser label in place

PCBA properly aligned in plastic case.
No bent or warped EMI shields
EMI  Shields  properly  placed inside the case.
CD  cover shall open without any friction when eject knob is pressed.
CD cover when opened, shall stand in opened position until closed by
                                                          the user
CD shall stop spinning when cd cover is opened.

### 5.5  Packout  Inspection

All  items  listed  on  the  BOM  shall  be  included as described  on the associated

assembly  drawings. The  gift  box  shall  be  weighed  to  check  if  any  item is

missing  inside  the  box.

This ends the final system test.

### 5.6  Report

Failure data shall be collected on all nonconforming units by failure code.
Repair actions associated with failure code shall also be collected. This
information shall be reported to Atari monthly. In addition, information on
top 10 test failures and top 10 repair actions shall be reported weekly to Atari

in Pareto chart format.

## 5.7 Fully Automated Functional Test Error Messages

Automated Test                                  Failure Message or State

1.  Door open/closed switch                     no test start
2.  Data Integrity                              (type) failed
3.  Audio playback                              DSA error condition
4.  Multiple seek speed test                    DSA error condition
5.  Verify CIRC detection circuit               no SAA7345 MISC output
6.  Subcode R-W channels                        Subcode R-W not valid
7.  EEPROM read/write                           failed
8.  Subcode Q                                   no subcode Q on V4

# 6.0  Diagnostic Tests

Any test contained in the Final Systems Test can be executed manually as a

diagnostic test, when the UUT is connected to a  serial data terminal or PC emulating a  serial data terminal. The Static behavior of  servo test  and  the Gain tests are not available as part of  the production tests but can be invoked to trouble-shoot defective units in diagnostic mode

## 6.1 Static behavior of servo drivers

These tests are performed with power on the circuit, but no disc in the drive.

### 6.1.1  Focus driver offset voltage

Measure the voltage between pin 2 (TP366) and pin 3(TP367) on JP3 (flex circuit

connector) and verify that...

$V_{focus\ 1}$   = 0.00 Volts, +/- 0.450 V

### 6.1.2  Radial driver offset voltage

Measure  the  voltage between pin 1(TP369) and pin 4(TP368) on JP3(flex circuit

connector)  and  verify  that...

$$V_{radial\ 1}\ =\ 0.00\ Volts\ ,\ +/-\ 0.450\ V$$

### 6.1.3  Sled driver offset voltage

Measure the voltage between pin 5(TP364) and pin 6(TP365) on JP4(motor cable connector)  and  verify  that...

$$V_{sled}\ =\ 0.00\ Volts\ ,\ +/-\ 0.450\ V$$

### 6.1.4  Spindle driver offset voltage

Measure the voltage between pin 3(TP362) and pin 4(TP363) on JP4(motor cable connector) and  verify  that...

$$V_{motor\ 1}\ =\ 0.00\ Volts\ ,\ +/-\ 0.450\ V$$

## 6.2  Gain tests

**Note that the following 3 gain tests can damage the circuit if run for more than 5   seconds. The '!! ' preceding each test is a reminder of this fact.**

### 6.2.1  !!  Focus driver gain

Apply  3  volts  to  TP86 and measure the voltage between pin 2(TP366) and pin  3 (TP367)  on  JP3  ( flex circuit connector )  and  verify  that....

$$V_{focus\ 2}\ =\ 0.780\ Volts,\ +/-\ 20\%$$

### 6.2.2  !!  Radial driver gain

Apply  3  volts to TP87 and measure the voltage between pin 1 (TP369) and pin  4 (TP368) on  JP3  ( flex  circuit  connector )  and  verify  that....

$$V_{radial\ 2}\ =\ 0.780\ Volts,\ +/-\ 20\%$$

### 6.2.3  !!  Spindle driver gain

Apply 3 volts to TP84 and 2 volts to TP 85 and then measure the voltage between pin 3(TP362 )and pin 4(TP363) on  JP4 ( motor cable connector ) and verify that....

$$V_{motor\,2} = 0.780 \text{ Volts}, \ +/- 20\%$$

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### 6.3.1  Door Open/closed detection

The  CD  Module  top  lid  has  a  contact  switch  that  grounds  a  signal  wire  to  Butch ( ASIC at ref loc U9 ). At test  start,  the  lid  must  be  closed. If  the  lid  is  not  closed  no  further  tests  may  be  conducted  on  the  UUT.

|  Failure Condition | State or error code |
| --- | --- |
| Lid switch not connected | UUT held in reset |

### 6.3.2  Data Integrity

The drive  is  commanded  to  read  a  series  of  tracks on  the  disc, in  various  play command  formats.  The  track  data  are  verified  algorithmically.  Any  data

errors  cause  a  test  failure.  Any  drive  error  will  cause a  test  failure.

| Failure Condition | State or error code |
| --- | --- |
| Drive Error | DSA error condition |
| Data Err | "failed" message |

### 6.3.3  Audio Playback

The  drive  is  commanded  to  play  an  inner  audio  track, an  outer audio track, and  intermediate  tracks  containing  intentional  errors  and  defects. The  drive

must  track  through  these  without  errors.  Any  drive  error  will  cause  a test failure.

| Failure  Condition | State or error code |
| --- | --- |
| Drive error | DSA error condition |

### 6.3.4  Multiple seek speed test

The drive is commanded to seek between a set of target -times on  the  disc  while a  timer  is  running. The test must  complete  within the specified time, or the  test

fails.  Any  drive  error  will  also  cause  a  test  failure.

| Failure condition | State or error code |
| --- | --- |
| Drive Error | DSA  error condition |
| Excessive time | Seek timeout message |

### 6.3.5  Verify CIRC detection circuit

The area  of the test disc with a known  defect is played repeatedly while the count

of  anticipated errors is  matched  to  the  actual  count. A difference  will  cause a

failure,  as  will a count of  zero. Any  unanticipated drive errors  will also cause a

test  failure.

| Failure condition | State or error code |
|---|---|
| Drive Error | DSA error condition |
| Missed CIRC | MISC pin error message |

### 6.3.6  Subcode R-W Channels

Subcode  from  the  R  through  W  channels  is read from a predetermined area of the disc with a known pattern. Any deviation  from  this  pattern  causes  a  failure.
Any  drive  error  also  causes  a  failure.

| Failure condition | State or error code |
|---|---|
| Drive error | DSA error condition |
| R-W subcode error | R-W subcode error |

### 6.3.7  EEPROM read/write

The EEPROM on the CD Module is written with a known pattern, and  then  read  back.  Any  differences  cause  a  failure.

| Failure condition | State or error code |
|---|---|
| IC wrong | System hangs |
| IC missing or defective | "failed" message |

### 6.3.8  Subcode Q

Subcodes from  the  Q  channel  is  read  from  the  disc. If the  subcode  is  not incrementing  as  it  should when the disc plays, the test fails.  Any drive error also

causes  a  failure.

| Failure condition | Extended error code |
|---|---|
| Drive  Error | DSA Error Condition |
| Q subcode error | no subcode Q on V4 |

## APPENDIX  A

## PCBA FUNCTIONAL TEST FIXTURE SPECIFICATION

The bed-of-nails ( PCBA) functional test fixture shall incorporate various system components and provide connections from these components to the Unit Under Test (UUT) PCBA.

### 9VDC power

The UUT connector JP12 shall connect to a 9V DC power source with a DC current meter **( with peak- holding setup required !)** connected in series with the positive side of the DC input power, JP12 pin 2 (TP65). 9VDC power shall be provided to the Jaguar console PCBA by two Atari AC adapters.

### 108 pin connector

The UUT 108 pin connector shall interface to a Jaguar console PCBA, which will be part of the test fixture and contain the test software. This connection may be provided to the UUT through a CD-ROM extender card to J801.

### +5VDC regulator output

The UUT jumper JP224 must be left out and a DC current meter connected in series between JP224 pin 1 (TP9) and JP224 pin 2 (TP337).

### +7VDC regulator output

The UUT jumper JP223 must be left out and a peak-holding type DC current meter connected in series between JP223 pin 1 (TP63) and JP223 pin 2 (TP334).

### CDM12 motor

The UUT connector JP4 must connect to a CDM12 motor. The CDM12 shall be a permanent part of the test fixture unless the system CDM12 is installed on the UUT PCBA prior to test and shipped as a complete assembly.

### CDM12 Laser

The UUT connector JP3 must connect to a CDM12 laser. The CDM12 shall be a permanent part of the test fixture unless the system CDM12 is installed on the UUT
PCBA prior to test and shipped as a complete assembly.

**BLER**

The UUT jumper between pin 1 (TP344) and pin 2 (TP346) of JP225 must be left out. The test fixture must short pin 2 (TP346) and pin 3 (TP343) of JP225. TP 375 (CDV4 signal) should be pulled high to +5V with a 4.7K 1/4W resistor. This enables the test software to measure the block error rate.

**JITTER**

The Jitter measurement shall be done on the UUT for inner and outer tracks of the CD ROM test disk. Test points TP34 [pin 8 of U8 (HFIN) ] and TP345 [pin 12 of
U8 (HFGND)] of the UUT shall be used for jitter measurements and corresponding
peak to peak voltage measurement. Provision to connect a CD jitter meter ( Leader
LJM 1851 CD Jitter Meter ) at above specified test points shall be provided on the test fixture.

**VOLTAGE MEASUREMENTS**

The test fixture shall have the capability to measure voltages at the following test
points on the UUT.

DC Voltage between TP60 (pin 17 & 18 of U4) and GND (pin 19 of U4)
DC Voltage between TP362 (pin 3 of JP4) and TP363 (pin 4 of JP4)

DC Voltmeters shall be attached to the test fixture to measure the voltages at the above specified test points.

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**APPENDIX B**

## STATIC  BURN-IN   SPECIFICATION

The  Static  Burn-in  facility  will  include  a  burn-in  chamber  operating  at  a  constant
temperature  of  50 degree C  and  power  distribution  network. The  power  distribution
network  will  provide  dual  DC  supply  voltage  of  9V  and  5V  to power  the  PCBA.
The  9V  supply  will  power  the  PCBA   through  power  jack  JP12.

The 5V  is  supplied  to the PCBA  through  an   interconnect  pcb ( provided  by Atari)
plugged  into connector J801  of  the  PCBA.

**Specification for interconnect PCB.**

The  interconnect  card  used  in  static  burn  in  is  a  PCB  that  can  be  inserted  into
connector  J801 of  CD ROM  player  PCBA  (700037)  and   supplies  +5V  to PCBA
to  turn  ON   the  voltage   regulators  U5   and  U13.  The  interconnect  card  has  no
components.

The  +5V is  at  pin 38A  and ground is at  pin  21A  of the adapter  card.  The  5V can
be  wired  directly  to  the  card  from  a  high  capacity  power  supply . The  power
supply should be OFF  before inserting  the card into the PCBA  and at  the  the  end
of
the test the  power supply should  be  turned  OFF  before  removing  the card from
the
PCBA .